FIG. 1

FIRST EMBODIMENT

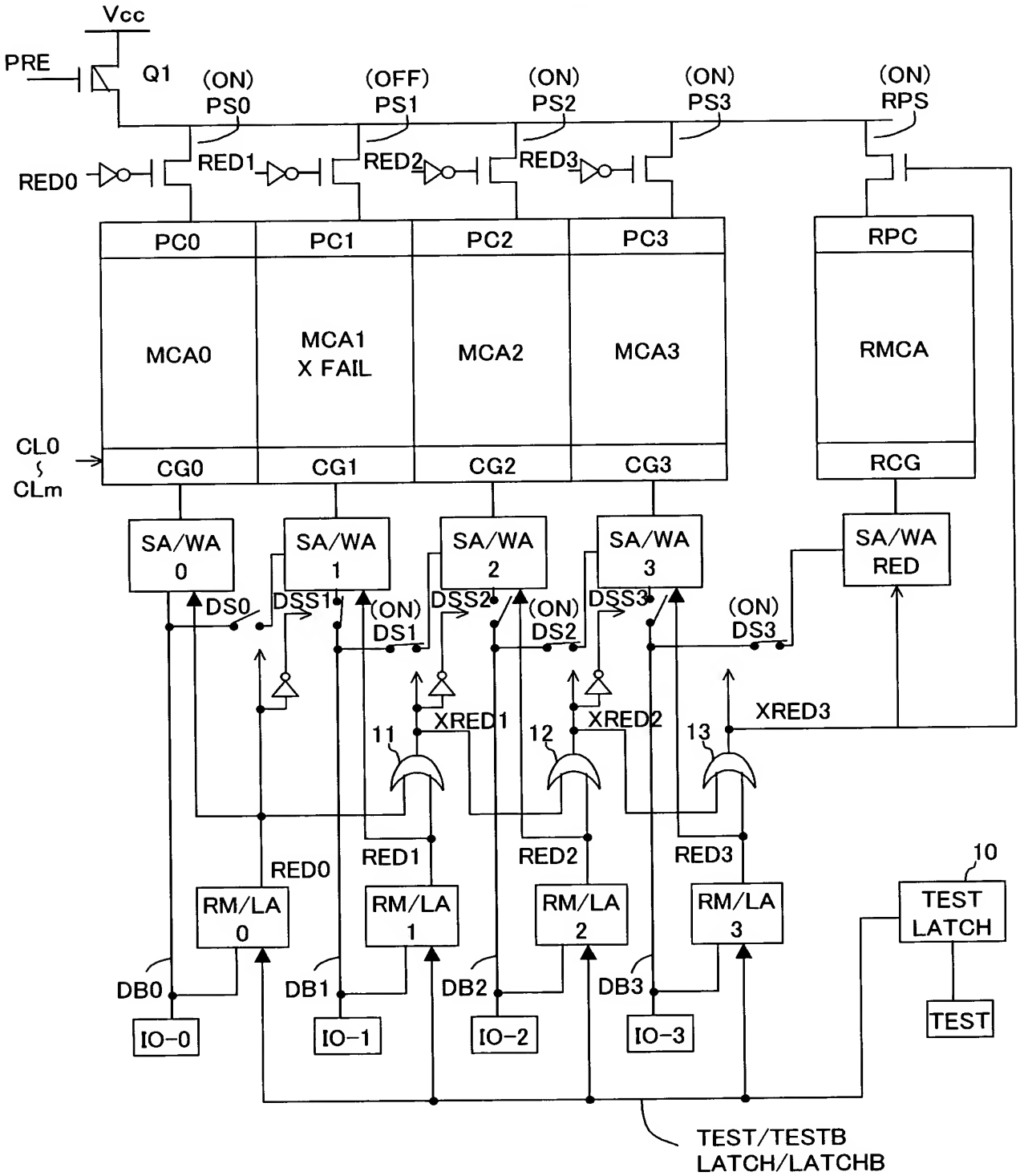


FIG. 2

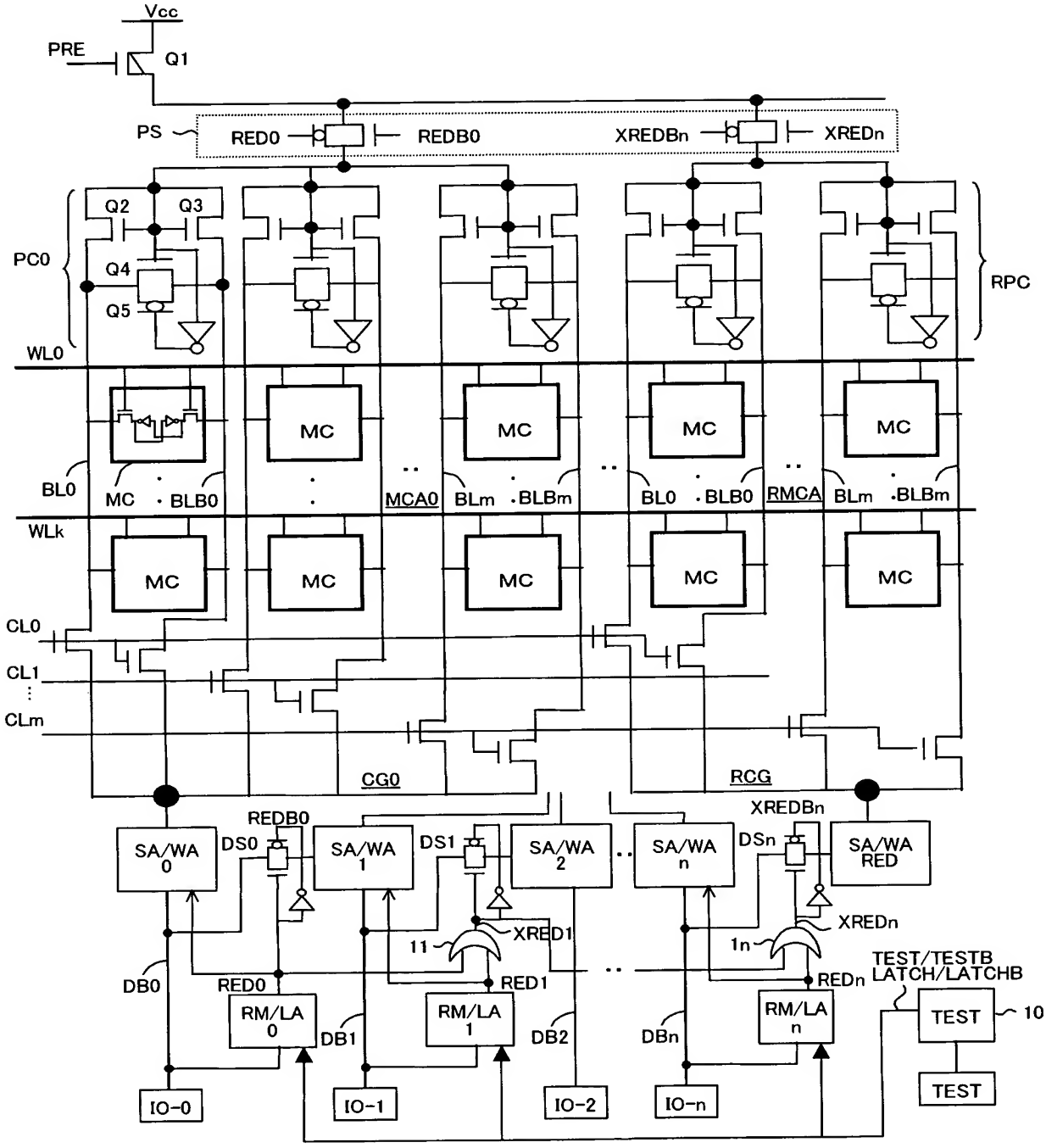

Vcc
PRE
Q1
PS
RED0
REDB0
XREDBn
XREDn
Q2
Q3
Q4
Q5
PC0
RPC
WL0
WLk
MC
BL0
BLB0
BLm
BLBm
MCA0
RMCA
CL0
CL1
CLm
CG0
RCG
REDB0
XREDBn
SA/WA 0
SA/WA 1
SA/WA 2
SA/WA n
SA/WA RED
DS0
DS1
DSn
XRED1
XREDn
11
1n
DB0
RED0
RED1
REDn
RM/LA 0
RM/LA 1
RM/LA n
DB1
DB2
DBn
TEST/TESTB
LATCH/LATCHB
TEST
10
IO-0
IO-1
IO-2
IO-n

FIG. 3

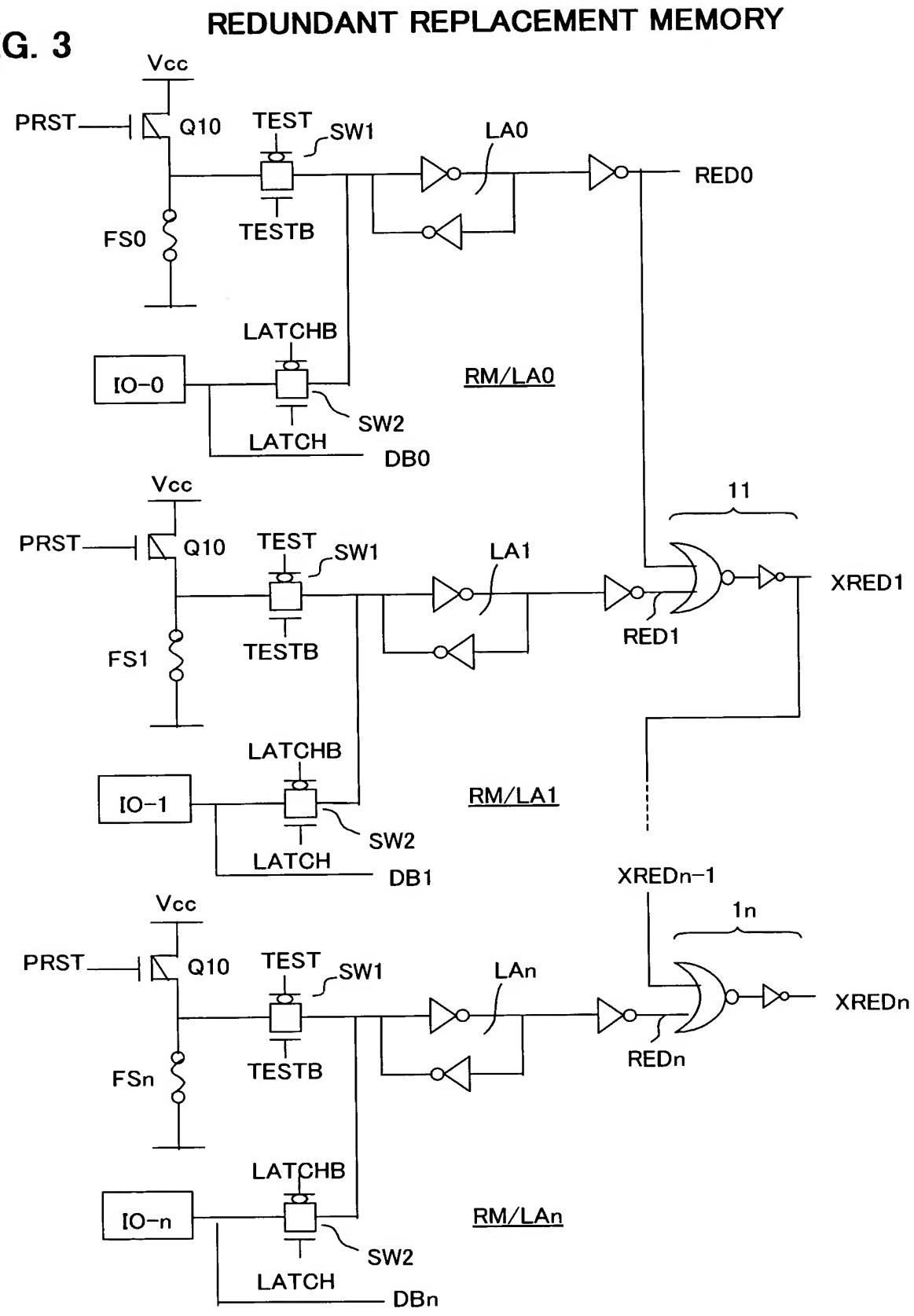

REDUNDANT REPLACEMENT MEMORY
Vcc
PRST
Q10
TEST
SW1
LA0
RED0
FS0
TESTB
LATCHB
IO-0
RM/LA0
SW2
LATCH
DB0
11
LA1
XRED1
RED1
FS1
IO-1
RM/LA1
DB1
XREDn-1
1n
LAn
XREDn
REDn
FSn
IO-n
RM/LAn
DBn

FIG. 4

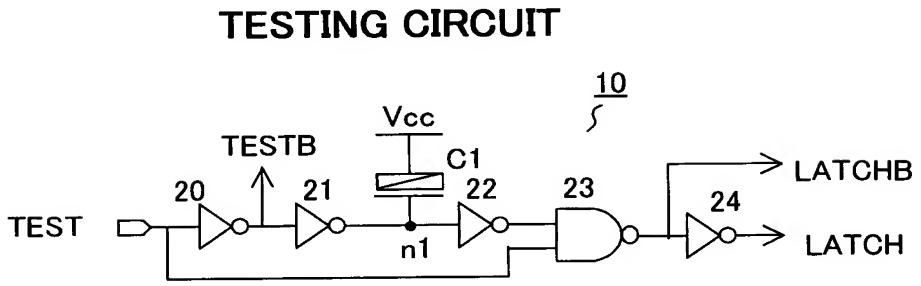

TESTING CIRCUIT
10
Vcc
TESTB
C1
20
21
22
23
24
TEST
n1
LATCHB
LATCH

FIG. 5

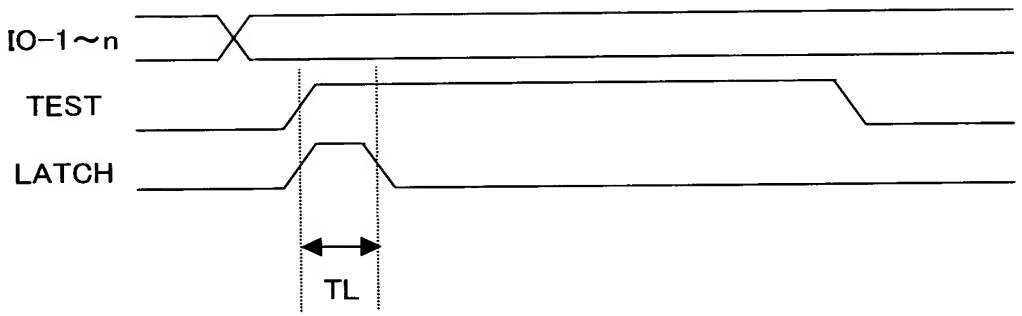
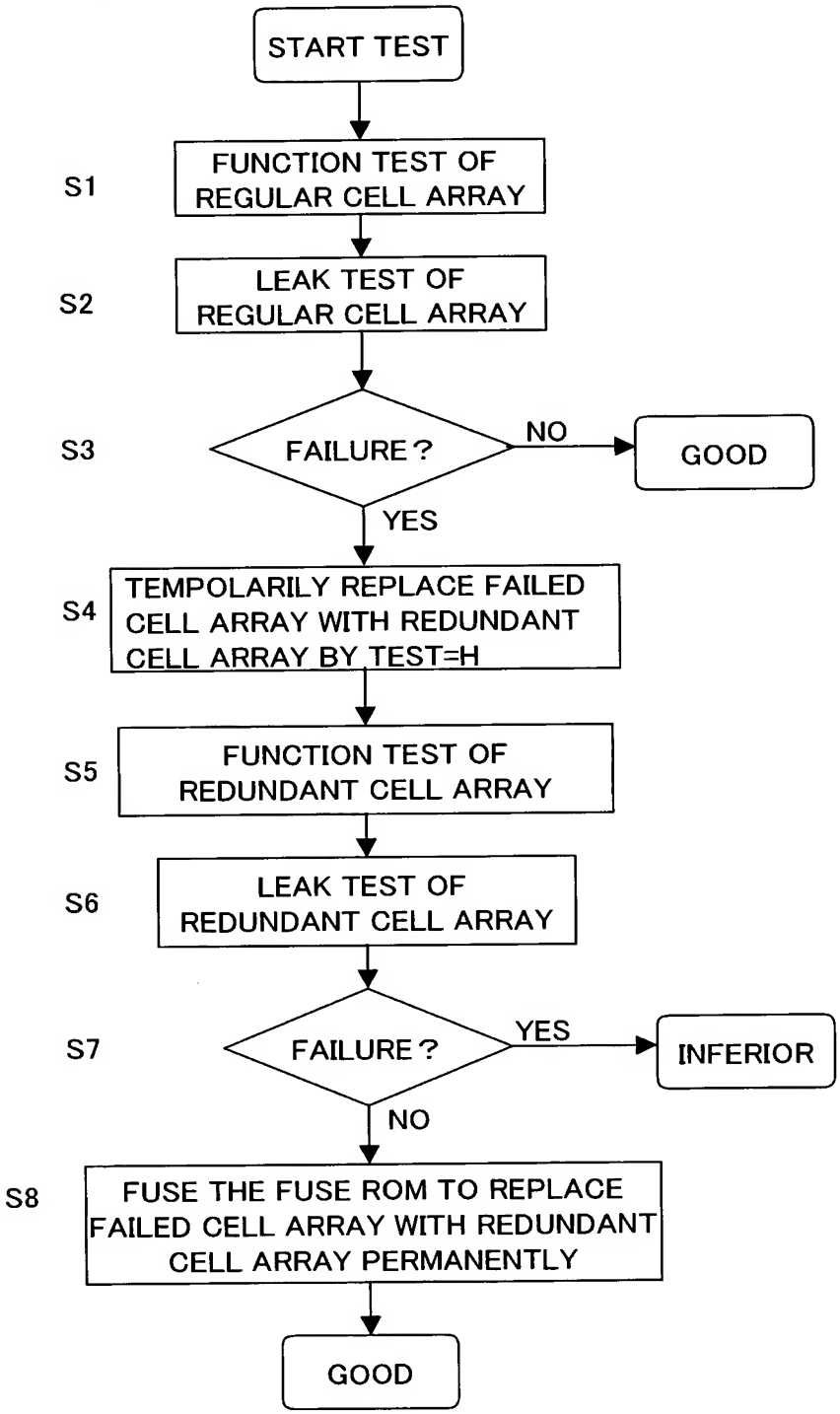

IO-1~n
TEST
LATCH
TL

FIG. 6


START TEST
S1
FUNCTION TEST OF REGULAR CELL ARRAY
S2
LEAK TEST OF REGULAR CELL ARRAY
S3
FAILURE?
NO
GOOD
YES
S4
TEMPOLARILY REPLACE FAILED CELL ARRAY WITH REDUNDANT CELL ARRAY BY TEST=H
S5
FUNCTION TEST OF REDUNDANT CELL ARRAY
S6
LEAK TEST OF REDUNDANT CELL ARRAY
S7
FAILURE?
YES
INFERIOR
NO
S8
FUSE THE FUSE ROM TO REPLACE FAILED CELL ARRAY WITH REDUNDANT CELL ARRAY PERMANENTLY
GOOD

Title: MEMORY CIRCUIT WITH REDUNDANT MEMORY CELL ARRAY ALLOWING SIMPLIFIED SHIPMENT TESTS AND REDUCED POWER CONSUMPTIONS
Inventor: TANISHIMA et al.
Application No. New
Docket No. 108066-00096

FIG. 7

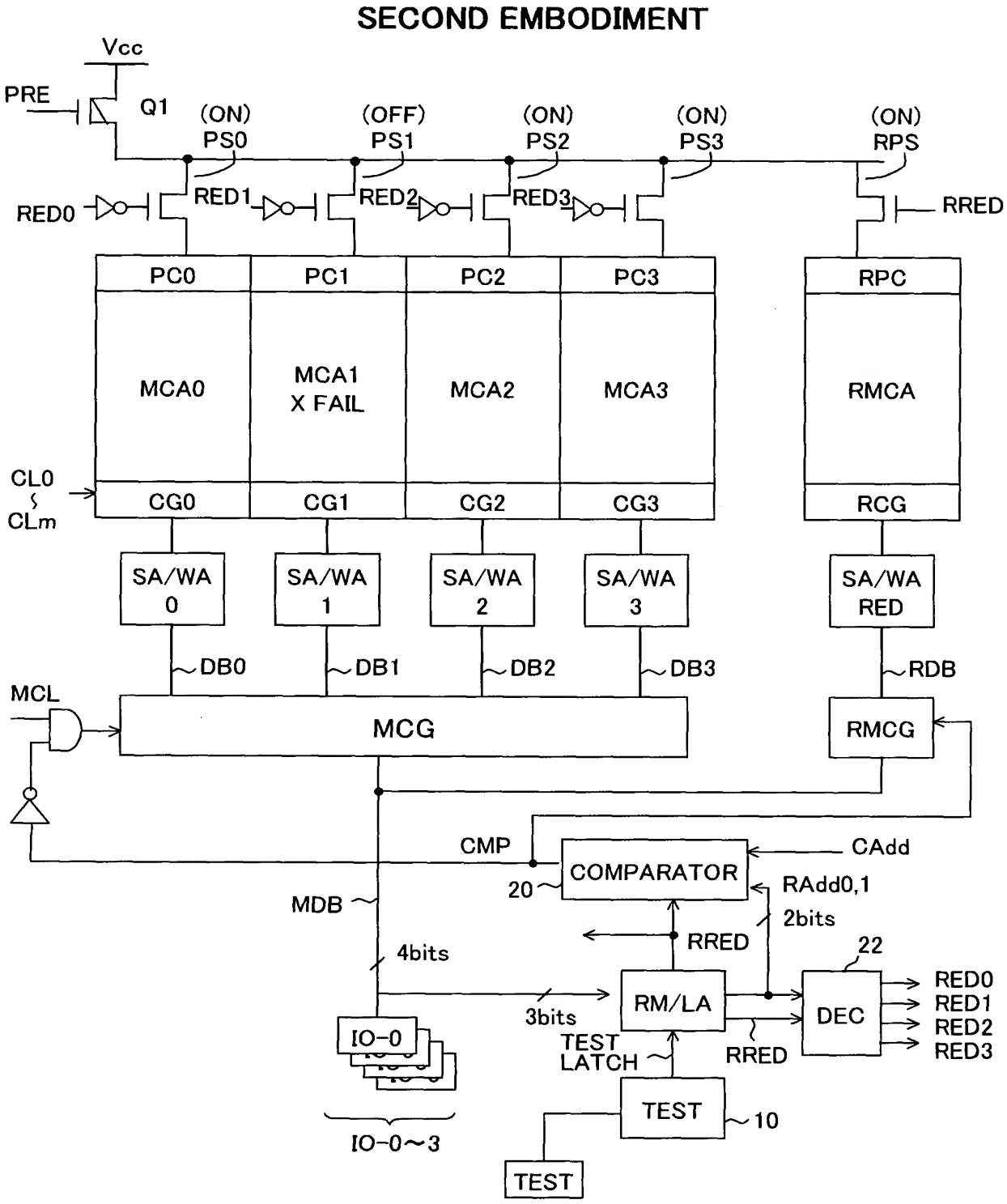
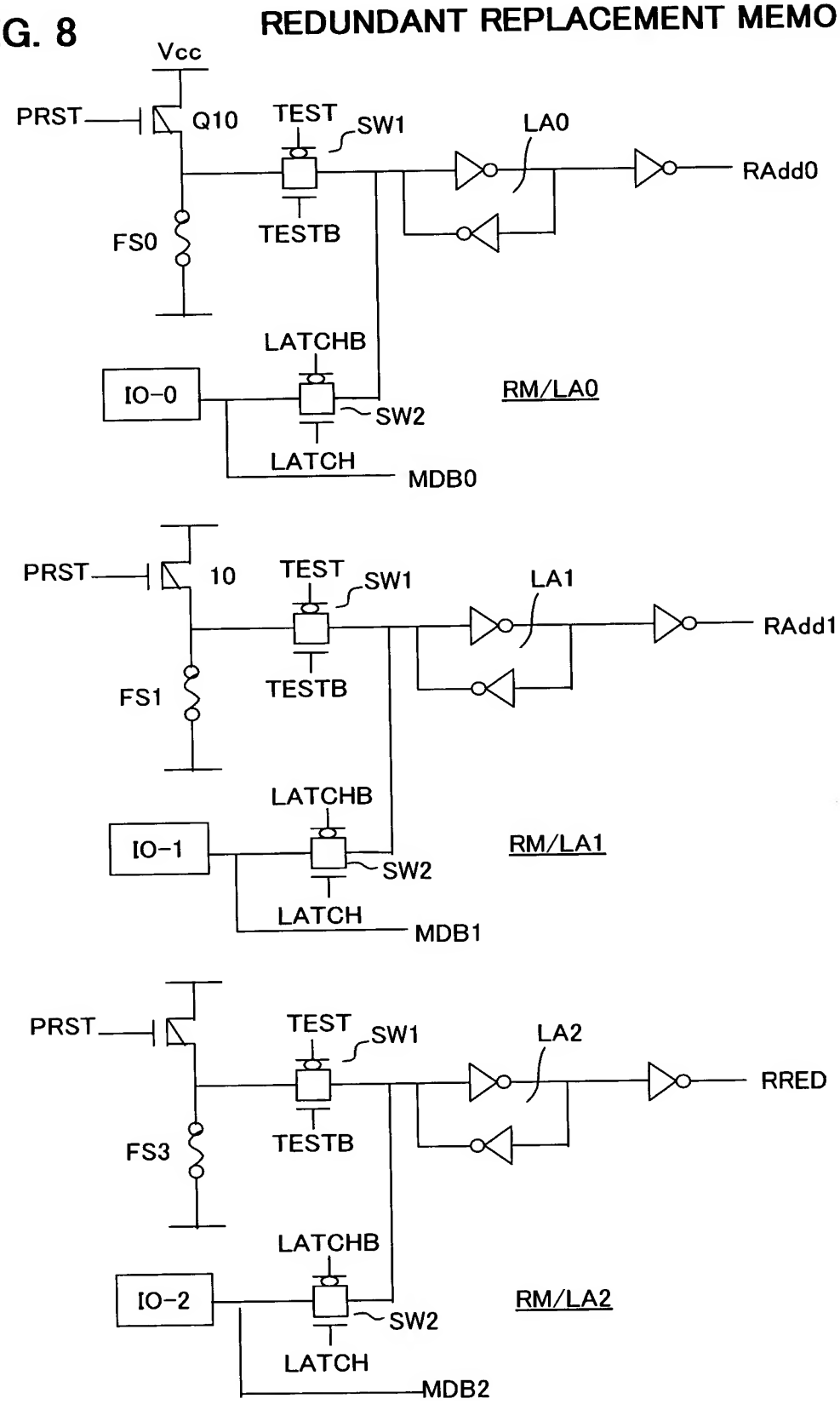


FIG. 8


REDUNDANT REPLACEMENT MEMORY
Vcc
PRST
Q10
TEST
SW1
LA0
RAdd0
FS0
TESTB
LATCHB
IO-0
RM/LA0
SW2
LATCH
MDB0
PRST
10
TEST
SW1
LA1
RAdd1
FS1
TESTB
LATCHB
IO-1
RM/LA1
SW2
LATCH
MDB1
PRST
TEST
SW1
LA2
RRED
FS3
TESTB
LATCHB
IO-2
RM/LA2
SW2
LATCH
MDB2